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10/764,484	01/27/2004	Atsuhiro Mori	61282-059	6279

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,484	MORI, ATSUHIRO	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/2/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2 July 2007 has been entered.

Status of Claims

2. Claims 1-7 are pending in the Application.

Claims 1, 2, 5 and 6 are amended.

Claims 1-7 are rejected.

Response to Amendment

3. Applicant's amendments and arguments filed on 2 July 2007 in response to the office action mailed on 30 March 2007 have been fully considered, but they are moot in view of the new grounds of rejection necessitated by amendment.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-6 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As for claim 1, there is no support in the original disclosure for the newly added limitation "the access arranging means further causing the clock signal to the second data input/output means not to be stopped when an access of the first data input/output means to the data storing means is generated but an access of the second data input/output means to the data storing means is not generated." By referring to Applicant's Fig. 2 of the original disclosure, the aforementioned scenario recited in the instant claim appears to be consistent with the left leg of the flow chart provided (i.e. S200 to S201 to S202 (e.g. access request only to the first I/O device)). By traversing this path, it is clear that the clock to the second I/O device is stopped and subsequently restarted (i.e. S205 and S207), despite Applicant's recitation in the claim otherwise. As such, Applicant's instant claim directly contradicts the system's operation as disclosed by this figure.

As for claim 2, there is no support in the original disclosure for the newly added limitation, "wherein a wait request signal is not generated if an access of the input/output control means to the built-in memory is generated by an access of the processor to the built-in memory is not generated." By referring to Applicant's Fig. 5 of

the original disclosure, the aforementioned scenario recited in the instant claim appears to be consistent with the left leg of the flow chart provided (i.e. S500 to S501 to S502 (e.g. access request only to the external I/O device)). By traversing this path, it is clear that the clock to the processor is stopped and subsequently restarted (i.e. S505 and S507), despite Applicant's recitation in the claim otherwise. As such, Applicant's instant claim directly contradicts the system's operation as disclosed by this figure.

Claims 5 and 6 are rejected based on the same rationale as claims 1 and 2 respectively.

Claims 3 and 4 further limit claim 2, therefore they too are rejected for inheriting the deficiencies of claim 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fadavi-Ardekani et al. (US Patent 6,499,087 B1), hereinafter Fadavi-Ardekani, and in further view of Smith (US Patent 4,847,757).

As for claim 1, Fadavi-Ardekani teaches an information processing apparatus comprising:

data storing means (Fig. 1, element 200);

first and second data input/output means for giving access to the data storing means (Fig. 1, elements 100 and 104);

clock generating means for supplying a clock signal to the first and second data input/output means (Fig. 1 depicts clock signals between the agents and the switch, and likewise between the switch and the memory);

switching means for switching access of the first data input/output means or the second data input/output means to the data storing means (Fig. 1, element 102); and

access arranging means for causing the clock signal to the second data input/output means to be stopped and not allowing the second data input/output means to access the data storing means; for executing the access of the first data input/output means earlier than the second data input/output means when a contention of the access of the first data input/output means and the second data input/output means to the data storing means is generated, and for starting the access of the second data input/output means after the access of the first data input/output means is ended (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other agent to access the memory. The wait state is generated to avoid contention among the multiple agents. Once one agent completes access, the other agent can access the memory, col. 1, line 61 through col. 2, line 10).

Despite these teachings, Fadavi-Ardekani fails to specifically teach the clock generating means as supplying the clock *to* (emphasis added) the second data input/output means. Rather, Fadavi-Ardekani teaches the agent itself as generating the clock and sending it to the memory. Additionally, Fadavi-Ardekani fails to teach the access arranging means further causing the clock signal to the second data input/output means not to be stopped when an access of the first data input/output means to the data storing means is generated but an access of the second data input/output means to the data storing means is not generated as recited in this claim.

Smith however teaches interleaved access to a global memory in which wait states are generated to arbitrate access of multiple I/O devices to a global memory – col. 5, lines 35-49. More specifically, access is arbitrated and interleaved via global address and data busses (e.g. address, data and clocking are external to internal arbitration). Wait states are generated only when contention between competing I/O resources attempt to access the shared resource – col. 5, line 35 through col. 6, line 2, see also abstract). In other words, a wait state for access from a second I/O resource to a shared memory occurs only when more than one resource attempts to access the shared memory.

As for claim 2, Fadavi-Ardekani teaches an information processing apparatus comprising:

a built-in memory (Fig. 1, element 200);

a processor for processing data stored in the built-in memory (Fig. 1, element 100);

clock generating means for supplying a clock signal from the processor (Fig. 1 depicts clock signals between the agents and the switch, and likewise between the switch and the memory);

input/output control means for executing access to the built-in memory from an external control device (Fig. 1, element 104 – super agent is capable of executing access to the memory); and

access arranging means for causing the clock signal to be stopped and carrying out access of the input/output control means with a priority when a contention of access of the processor and the input/output control means to the built-in memory is generated (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other agent to access the memory. The wait state is generated to avoid contention among the multiple agents. Once one agent completes access, the other agent can access the memory - col. 1, line 61 through col. 2, line 10. Also note Fadavi-Ardekani teaches designating a super agent which has priority over the other agent(s) – col. 3, lines 27-67 – a wait request signal is inherit to Fadavi-Ardekani's system in order for it to properly enable the agent that does not win access to the memory to enter in the wait state).

Despite these teachings, Fadavi-Ardekani fails to specifically teach the clock generating means as supplying the clock *to* (emphasis added) the processor. Rather, Fadavi-Ardekani teaches the agent itself as generating the clock and sending it to the memory. Additionally, Fadavi-Ardekani fails to teach wherein a wait request signal is

not generated if an access of the input/output control means to the built-in memory is generated by an access of the processor to the built-in memory is not generated as recited in this claim.

Smith however teaches interleaved access to a global memory in which wait states are generated to arbitrate access of multiple I/O devices to a global memory – col. 5, lines 35-49. More specifically, access is arbitrated and interleaved via global address and data busses (e.g. address, data and clocking are external to internal arbitration). Wait states are generated only when contention between competing I/O resources attempt to access the shared resource – col. 5, line 35 through col. 6, line 2, see also abstract). In other words, a wait state for access from a processor to a shared memory occurs only when more than one resource attempts to access the shared memory.

As for claim 5, Fadavi-Ardekani teaches memory access arranging method of an information processing apparatus including data storing means and first and second data input/output means for giving access to the data storing means, comprising the steps of:

causing a clock signal for the second data input/output means to be stopped and not allowing the second data input/output means to access the data storing means when a contention of the access of the first data input/output means and the second data input/output means to the data storing means is generated (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other agent to access the memory. The wait state is generated to

avoid contention among the multiple agents. Once one agent completes access, the other agent can access the memory. col. 1, line 61 through col. 2, line 10);

executing the access of the first data input/output means earlier than the second data input/output means (the super agent can access the memory while the other agents must wait, or similarly if two non-super agents contend for access, one will be granted access while the other will be required to wait – col. 3, lines 57-67); and

canceling the stop of the clock signal of the second data input/output means after ending the access of the first data input/output means, and executing the access of the second data input/output means (once the first agent has completed access, the wait state is released and the other agent is permitted to access the memory – col. 4, lines 16-53).

Despite these teachings, Fadavi-Ardekani fails to specifically teach the clock generating means as supplying the clock *to* (emphasis added) the second data input/output means. Rather, Fadavi-Ardekani teaches the agent itself as generating the clock and sending it to the memory. Additionally, Fadavi-Ardekani fails to teach the access arranging means further causing the clock signal to the second data input/output means not to be stopped when an access of the first data input/output means to the data storing means is generated but an access of the second data input/output means to the data storing means is not generated as recited in this claim.

Smith however teaches interleaved access to a global memory in which wait states are generated to arbitrate access of multiple I/O devices to a global memory – col. 5, lines 35-49. More specifically, access is arbitrated and interleaved via global

address and data busses (e.g. address, data and clocking are external to internal arbitration). Wait states are generated only when contention between competing I/O resources attempt to access the shared resource – col. 5, line 35 through col. 6, line 2, see also abstract). In other words, a wait state for access from a second I/O resource to a shared memory occurs only when more than one resource attempts to access the shared memory.

As for claim 6, Fadavi-Ardekani teaches a memory access arranging method of an information processing apparatus including a processor for carrying out a pipeline processing over an instruction, a memory provided in the processor, and input/output control means for executing access to the memory with a higher priority than the processor, comprising the steps of:

causing a clock signal supplied to the processor to wait when a contention of access of the processor and the input/output control means to the memory is generated (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other agent to access the memory. The wait state is generated to avoid contention among the multiple agents. Once one agent completes access, the other agent can access the memory - col. 1, line 61 through col. 2, line 10. Also note Fadavi-Ardekani teaches designating a super agent which has priority over the other agent(s) – col. 3, lines 27-67 – a wait request signal is inherit to Fadavi-Ardekani's system in order for it to properly enable the agent that does not win access to the memory to enter in the wait state);

switching the access of the processor to the access of the input/output control means to the memory (arbiter - Fig. 1, element 102 control which agents can access the memory); and

canceling the wait request signal of the processor after ending the access of the input/output control means to the memory, and executing the access of the processor to the memory (once the first agent has completed access, the wait state is released and the other agent is permitted to access the memory – col. 4, lines 16-53).

Despite these teachings, Fadavi-Ardekani fails to teach wherein a wait request signal is not generated if an access of the input/output control means to the built-in memory is generated by an access of the processor to the built-in memory is not generated as recited in this claim.

Smith however teaches interleaved access to a global memory in which wait states are generated to arbitrate access of multiple I/O devices to a global memory – col. 5, lines 35-49. More specifically, access is arbitrated and interleaved via global address and data busses (e.g. address, data and clocking are external to internal arbitration). Wait states are generated only when contention between competing I/O resources attempt to access the shared resource – col. 5, line 35 through col. 6, line 2, see also abstract). In other words, a wait state for access from a second I/O resource to a shared memory occurs only when more than one resource attempts to access the shared memory.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fadavi-Ardekani to further include Smith's system of interleaved access to global memory via wait states into his own system of synchronous memory sharing based on cycle stealing. By doing so, Fadavi-Ardekani would benefit by having a more efficient memory system (e.g. low cost, high speed, implemented with a simplified circuit implementation) that allows both higher and lower priority processors to access his shared memory as taught by Smith in col. 1, lines 37-60.

As for claim 3, Fadavi-Ardekani teaches the information processing apparatus according to claim 2, further comprising

selecting means for switching the access of the processor and the input/output control means to the built-in memory (Fig. 1, element 102),

wherein the access arranging means outputs a control signal to the selecting means when a request for the access of the input/output control means to the built-in memory is generated during the access of the processor to the built-in memory (each agent is connected to the switch/arbiter via the ADC (address, data, and control) lines which is used to permitted access to the memory via one and only one agent – see Fig. 1. When a super agent requires access, it is able to obtain uncontested priority without requiring the arbiter to grant access – col. 1, lines 40-67. In other words, the super agent asserts control over the arbiter to grant access to the memory), and

the selecting means receiving the control signal switches the access of the processor to the access of the input/output control means to the built-in memory

(the switch/arbiter (Fig. 1, element 102) is capable of arbitrating access between the two agents, and selectively permitting control to one based on priority).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fadavi-Ardekani (US Patent 6,499,087 B1) and Smith (US Patent 4,847,757) as applied to claim 2 above, and in further view of Peters (US Patent 6,065,102).

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As for claim 4, though the combined disclosure of Fadavi-Ardekani and Smith meet all the limitations of claim 2, they fail to specifically teach, holding means for holding read data output from the built-in memory before a wait operation of the processor during the wait operation of the processor, wherein the access arranging means switches read data to be supplied to the processor between the read data output from the built-in memory and the read data held by the holding means as recited in this claim.

Peters however teaches a fault tolerant multiple client memory arbitration system, which allows multiple clients to access data redundantly stored in two cache memories (col. 2, lines 53-65). In other words both the local cache memory and the redundant cache memory store the same data. The system further allows for the arbitration of access to either the local cache memory, or the mirrored cache memory. In other words, data can be extracted from alternative holding means (i.e. the mirrored cache) rather than the local cache itself depending on the status of the arbitration logic.

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Fadavi-Ardekani and Smith to further include

Peters multiple client arbitration system into his own system of synchronous memory sharing based on cycle stealing. By doing so, they would be able to improve the fault tolerance of their memory system by proving redundant storage as taught by Peters in col. 1, lines 23-45.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fadavi-Ardekani (US Patent 6,499,087 B1), in further view of Peters et al. (US Patent 6,065,102), hereinafter Peters.

As for claim 7, Fadavi-Ardekani teaches a memory access arranging method of an information processing apparatus having a processor for carrying out a pipeline processing over an instruction, a memory provided in the processor, input/output control means for executing access to the memory with a higher priority than the processor, and holding means for holding read data output from the memory before a wait operation of the processor during the wait operation of the processor, comprising the steps of:

> causing a clock signal supplied to the processor to be stopped (Fadavi-Ardekani teaches each agent as having it own unique clock. The clock of one agent must enter a wait state to allow the other agent to access the memory. The wait state is generated to avoid contention among the multiple agents. Once one agent completes access, the other agent can access the memory. col. 1, line 61 through col. 2, line 10);

executing the access of the input/output control means to the memory (the winning agent can access the memory once the arbiter grants access to the memory – col. 3, lines 26-67); and

canceling the stop of the clock signal of the processor after ending the access of the input/output control means to the memory, and restarting the access of the processor to the memory (once the first agent has completed access, the wait state is released and the other agent is permitted to access the memory – col. 4, lines 16-53).

Despite these teachings, Fadavi-Ardekani fails to teach holding the read data output from the memory in a holding means before the wait operation of the processor when a contention of read access of the input/output control means is generated. Additionally Fadavi-Ardekani fails to teach, supplying the data held in the holding means to the processor.

Peters however teaches a fault tolerant multiple client memory arbitration system which allows multiple clients to access data redundantly stored in two cache memories (col. 2, lines 53-65). In other words both the local cache memory and the redundant cache memory store the same data. The system further allows for the arbitration of access to either the local cache memory, or the mirrored cache memory. In other words, data can be extracted from alternative holding means (i.e. the mirrored cache) rather than the local cache itself depending on the status of the arbitration logic.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fadavi-Ardekani to further include Peters multiple client arbitration system

into his own system of synchronous memory sharing based on cycle stealing. By doing so, Fadavi-Ardekani would be able to improve the fault tolerance of his memory system by proving redundant storage as taught by Peters in col. 1, lines 23-45.

Response to Arguments

8. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new grounds of rejection discussed *supra*.

9. Applicant failed to overcome the previously asserted §103(a) rejection against claim 7 either through amendment or argument, therefore this rejection is maintained and restated above.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG S SOUGH
SUPERVISORY PATENT EXAMINER
10/29/07